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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,251	10/16/2001	Myung Sub Sim	K-0317	2253

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EXAMINER	
HO, THOMAS M	

ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 08/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,251	SIM, MYUNG SUB	
	Examiner	Art Unit	
	Thomas M. Ho	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4, 6-9, 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

KAMBIZ ZAND
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4, 6-9, 11-14 are pending.

2. The RCE of 7/10/06 has been received and entered.

Response to Arguments and Amendments

3. The Applicant has argued on page 2, paragraph 2:

Van Stralen does not teach or suggest all the features of independent claim 1. More specifically, independent claim 1 specifically recites storing the primarily decoded signals in a specific address space of a memory, interleaving the primarily decoded signals stored in the memory and storing the deinterleaved signals in the specific address space of the memory. Van Stralen does not teach or suggest these features. Van Stralen discloses a top code memory 16, a bottom code memory 20 and a probability estimate memory 24. However, there is no suggestion in Van Stralen for storing primarily decoded signals in a specific address space of a memory and also storing the deinterleaved signals in the specific address space of the memory. Merely because signals may be stored in one memory, this does not suggest storing both types of signals in a specific address space of a memory. See paragraphs [20]-[21] of the present specification, for example.

The Examiner contends however that term "specific address space" may refer to any part of the memory. An address space can be as simple as a single memory address, or a range or "space" within a greater memory construct.

The code is received from a transmission system and interleaved in item 18 and deinterleaved in Item 22. Thereafter, the signal is stored in the probability estimate memory which for purposes of examination has been interpreted to be the specific address space.

The Applicant has also argued on page 2, 3rd paragraph:
Additionally, Van Stralen does not teach or suggest that the interleaving, the secondarily decoding and the deinterleaving are implemented simultaneously. The Office Action asserts on pages 3-5 that Van Stralen does disclose "implemented simultaneously." The Office Action appears to make assertions without any factual basis in the reference.

The Examiner contends however that Figure 1 and (Column 3, lines 64 – Column 4, lines 4) clearly depicts interleaving, secondarily decoding and deinterleaving are performed simultaneously. Figure 1 shows multiple inputs simultaneously being processed and interleaved and deinterleaved. The diagram between each of the processing and memory modules would appear to indicate that while the Top code memory is receiving information from two inputs, the bottom code memory is receiving its signals from its own input. Additionally (Column 3, lines 64 – Column 4, lines 4) state that these codes are given in parallel. The Applicant's arguments simply allege that the Examiner's interpretation is not supported by the art without providing an

alternate explanation or counter evidence to how the module may function serially as opposed to simultaneously. For this reason, the Examiner has found Applicant's arguments unpersuasive.

The Applicant has also argued on page 3, paragraph 2:

The Office Action also asserts that Van Stralen's operation occurs on a stream of data and that turbo decoding is continuously processing a feed of data with all parts implemented simultaneously. Applicant respectfully submits that Van Stralen does not teach this alleged feature and that the Office Action's assertion is without any basis in the prior art.

The Examiner disagrees with the Applicant that continuous processing of a feed of data is without basis in the Van Stralen reference. It is the Examiner's position that any sequence of signal data may be referred to as a stream of data or a data stream. Even data that has been organized into a set of packets is often referred to as a stream of packets. A stream is commonly used term in the art used to refer to any incoming signal which is input over a given period of time. As for this feed of data occurring simultaneously, Figure 1 and (Column 3, lines 64 – Column 4, lines 4) disclose that the signals are given in parallel, which are then processed and interleaved in Figure 1.

Applicant also further expands this argument in page 3, last paragraph – page 4, first paragraph. Applicant's further arguments from pages 4-6 extend the arguments with respect to the limitations of claim 1 to the extent that claims 6, 11 and the other claims recite those limitations.

These arguments are addressed by the response to arguments above.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 6-9, 11-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Stralen et al., US patent 6304996.

In reference to claim 1:

Van Stralen et al. (Figure 1) discloses a method for performing turbo decoding, comprising:

- Primarily decoding signals received from a transmission system and storing the primarily decoded signals in a specific area of a memory, where the primary decoding signals are the signals of the top code parity data, the systematic data, and the bottom code parity data, and where the decoded signal is stored in the probability estimate memory.
- Interleaving the primarily decoded signals stored in the memory to change their order and secondarily decoding the interleaved signals, where the top and bottom signals are

interleaved (Column 3, line 64- Column 4, line 4) et seq. and then run through the map decoder. (Figure 1, Item 14)

- Deinterleaving the secondarily decoded signals and storing the deinterleaved signals in the specific address space. (Figure 1, Items 22, 24)

In reference to claim 2:

Van Stralen et al. discloses the method of claim 1, wherein the primary decoding and the secondary decoding are iterated n times using a Maximum A posteriori (MAP) algorithm, where the decoder is a MAP decoder. (Figure 1, Items 12, 14) & (Column 1, lines 45-50)

In reference to claim 3:

Van Stralen et al. discloses the method of claim 2, wherein the primary decoding is performed using a current transmission system signal of the transmission system signals and an (n-1)^n iteration signal of the secondarily decoded signals, where both the alpha and beta functions(understood in the art to as the forward and backward state probability functions) are recursively defined (Column 3, lines 10-45) , making their computations (n-1)n iteration signals of the secondarily decoded values.

In reference to claim 4:

Van Stralen et al. discloses the method of claim 1, wherein the secondary decoding is performed using the transmission system signals and the primarily decoded signals, where the secondary

decoding is the Map decoder (Figure 1, Item 14) and is performed using the original top code and bottom code signals.

In reference to claim 6:

Van Stralen et al. discloses a method for performing turbo decoding, comprising:

- Primarily decoding signals received from a transmission system and storing the primarily decoded signals into a specific address space of a memory. (Figure 1, Item 24)
- Interleaving the primarily decoded signals stored in the memory by an equation $E_i(k) = E(a(k))$, wherein k= 1,2,…,s, s is a code block size, and E(k) is a MAP decoded signal, and a(k) is a general interleaving function necessarily defined by an interleaver of a turbo decoder. (Figure 1, "interleavers") (Column 3, lines 64- Column 4, line 4) et seq.
- Secondarily decoding the interleaved signals in turn; (Figure 1, Item 14)
- Deinterleaving the secondarily decoded signals by an equation $E_d(a(k)) = E(k)$ wherein k = 1,2,…,s, s is the code block size and the E(k) is the MAP decoded signal; (Figure 1, Item 22) & (Column 3, lines 64- Column 4, line 4) et seq.
- Storing the deinterleaved signals in a predetermined region of the memory indicated by a(k). (Figure 1, Item 24) & (Column 3, lines 64- Column 4, line 4) et seq.

In reference to claim 11:

Van Stralen et al. discloses a method for performing turbo decoding, comprising:

- Primarily decoding composite signals comprising systematic symbols x_k,$(n-1)^{th}$ iteration extrinsic information, and parity symbols y_k; (Column 3, lines 10-45)
- Storing the primarily decoded composite signals in a specific address space of a memory; (Figure 1, Item 24)
- Interleaving the signals stored in the memory and secondarily decoding a second composite of the parity symbols y_k and the interleaved signals to generate n^{th} iteration extrinsic information. (Figure 1, "interleavers") (Column 3, lines 64- Column 4, line 4) et seq. & (Column 3, lines 10-45)
- Deinterleaving the secondarily decoded signals and storing the deinterleaved signals in the specific address space. (Figure 1, Items 22, 24)

Claims 7-9 are rejected for the same reasons as claims 2-4, respectively.

Claims 12-14 are rejected for the same reasons as claims 2-4, respectively.

Conclusion

7. Any inquiry concerning this communication from the examiner should be directed to Thomas M Ho whose telephone number is (571)272-3835. The examiner can normally be reached on M-F from 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on **(571)272-3799.**

The Examiner may also be reached through email through Thomas.Ho6@uspto.gov

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

General Information/Receptionist	Telephone: 571-272-2100	Fax: 571-273-8300
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TMH

August 14th, 2006

KAMBIZ ZAND
PRIMARY EXAMINER